NANO LETTERS

pubs.acs.org/NanoLett Letter

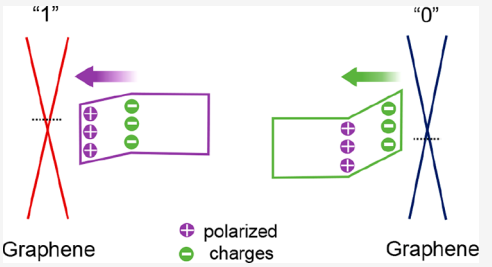
High-Performance Sliding Ferroelectric Transistor Based on Schottky Barrier Tuning

Renji Bian, Guiming Cao, Er Pan, Qing Liu,* Zefen Li, Lei Liang, Qingyun Wu, Lay Kee Ang, Wenwu Li,* Xiaoxu Zhao,* and Fucai Liu*

Cite This: *Nano Lett.* 2023, 23, 4595−4601 Read Online

ACCESS | Metrics & More | Article Recommendations | Supporting Information

ABSTRACT: Sliding ferroelectricity associated with interlayer translation is an excellent candidate for ferroelectric device miniaturization. However, the weak polarization gives rise to the poor performance of sliding ferroelectric transistors with a low on/off ratio and a narrow memory window, which restricts its practical application. To address the issue, we propose a facile strategy by regulating the Schottky barrier in sliding ferroelectric semiconductor transistors based on γ-InSe, in which a high performance with a large on/off ratio (10^6) and a wide memory window (4.5 V) was ultimately acquired. Additionally, the memory window of the device can be further modulated by electrostatic doping or light excitation. These results open up new ways for designing novel ferroelectric devices based on emerging sliding ferroelectricity.



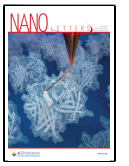
KEYWORDS: *sliding ferroelectric semiconductor, tunable Schottky barrier, high on/off ratio, electron doping*

Sliding ferroelectricity, which originates from the charge transfer between the asymmetric atomic layers in van der Waals materials, has been recently demonstrated.[1,2] The out-of-plane polarization can be switched by interlayer translation, distinct from the ion displacement in traditional ferroelectrics.[1−6] The intriguing switching mechanism makes sliding ferroelectricity promising for both fundamental research and device application. Benefiting from the weak interlayer dipole coupling, cumulative polarization states can be achieved in sliding ferroelectricity, which have been confirmed by the electrical transport measurement[7] and Kelvin probe force microscopy.[8] In sliding ferroelectrics, the polarization is confined to the interface, while the electric conductivity is provided by the migration of free carriers along the individual layer. The decoupling between ferroelectricity and conductivity in sliding ferroelectricity results in an abundance of physical phenomena such as a switchable superconductor,[9,10] switchable Moiré potentials,[11] and nonvolatile memory.[7] Such extraordinary physical phenomena associated with switchable electric dipoles exhibit great prospects in novel devices featured with in-memory computing. However, due to the weak polarization, the reported sliding ferroelectric transistors usually show a low on/off ratio, restricting the practical application of the revealed phenomena.[12]

To address the above drawbacks, a tunable Schottky barrier is introduced in sliding ferroelectric channel transistor (SFeCT), realizing the high performance with a wide memory window and a large on/off ratio. The γ-InSe was selected as a channel material, the ferroelectricity of which has been theoretically predicted.[1,13] Besides, it shows high carrier mobility exceeding 10^3 cm^2 V^{-1} s^{-1} at room temperature.[14,15] We experimentally demonstrated the sliding ferroelectricity in γ-InSe by using graphene as a sensor to monitor the switching of its polarization. The tunable Schottky barrier through electrically modulating the ferroelectric polarization results in a high-performance SFeCT based on γ-InSe, exhibiting a large memory window of 4.5 V and a high on/off ratio of 10^6. Surprisingly, it was found that the memory windows could even be tuned by the electric field of the top gate or light illumination, providing a novel way to develop ferroelectric multifunctional devices. Our work offers a promising avenue toward designing novel ferroelectric devices integrated with memory and computing functions.

Transmission electron microscopy was carried out to confirm the phase structure of InSe. As shown in Figure 1a, the hexagonal lattice spacing of 0.2 nm corresponds well with γ-polytype-layered InSe (a = b = 4.005 Å, c = 24.96 Å).[16] Theoretically, the direction of out-of-polarization is from top to bottom, originating from the nonsymmetric charge density distributions between neighboring layers, as shown in Figure 1b. The polarization can be flipped along upward orientation by interlayer sliding one-half bond of In−Se upon the application of an external electric field. The ferroelectric

Received: March 20, 2023
Revised: April 30, 2023
Published: May 8, 2023



https://doi.org/10.1021/acs.nanolett.3c01053
Nano Lett. 2023, 23, 4595−4601

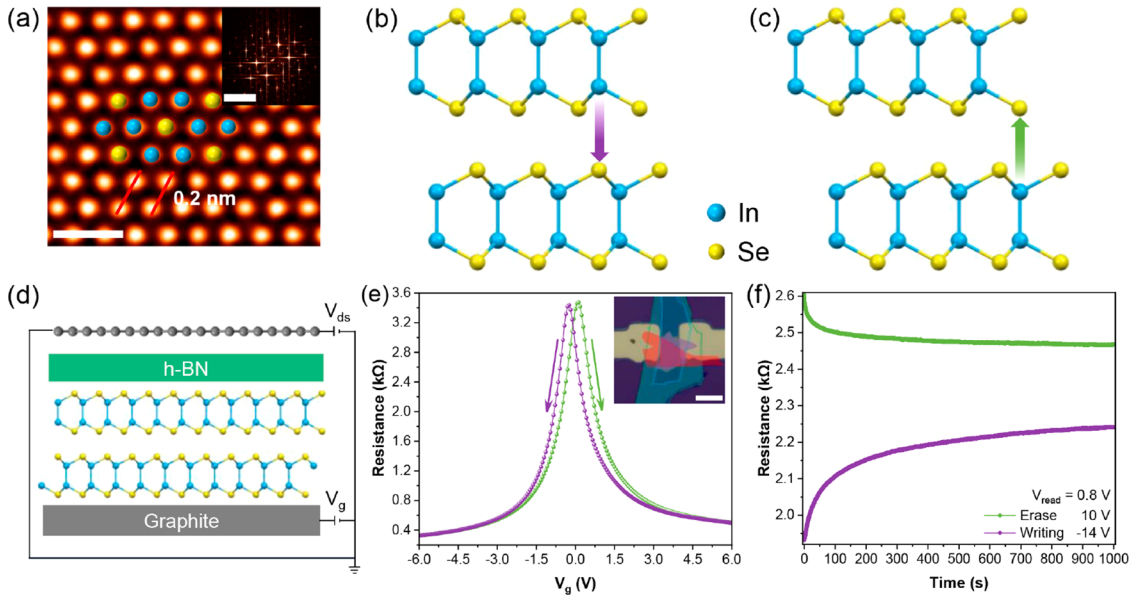


Figure 1. (a) Atomic-resolution STEM-ADF image of the thin γ-InSe flake. Scale bar is for 0.5 nm (inset: the FFT patterns, scale bar is for 10 nm^{-1}). (b) and (c) Side views of the γ-InSe crystal structure with switchable out-of-plane polarization by sliding a half of a unit cell. (d) The device structure, where γ-InSe acts as a dielectric layer. (e) Resistance of graphene as a function of back-gate voltage in the forward and backward scan directions. Inset: an optical image of the device, in which the γ-InSe acts as a dielectric layer (purple), and scale bar is for 10 μm. (f) Retention characteristics of different resistance states of graphene.

dipoles of sliding ferroelectricity can be indirectly monitored by adopting a graphene channel.[3,17,18] The device structure where graphene acts as a detector layer and γ-InSe plays a role as a ferroelectric layer is displayed in Figure 1d. An insulator layer of h-BN is introduced to improve the conductivity of graphene by reducing the phonon and Coulomb scattering.[19] From Figure 1e, the electrical characteristics of graphene show a typical butterfly-like hysteresis behavior associated with ferroelectricity when the gate voltage sweeps from −6 to 6 V and back to −6 V. Additionally, the retention properties of the ferroelectric polarization of γ-InSe have been further investigated under the gate writing (−14 V) and erasing (10 V), as shown in Figure 1f. It was found that the graphene resistances at both states change obviously during the first 100 s and then become nearly constant. After 1000 s, the dissimilarity of graphene resistance induced by the converse diploes is still distinguishable, suggesting there exists appreciable remnant polarization of sliding ferroelectricity in γ-InSe. It should be noted that the low ratio of resistance at different polarization states is attributed to the good conductance of graphene, where the extra carriers induced by ferroelectric dipoles are much smaller than the intrinsic carriers in graphene. As a contrast, a device where 2H-MoS_2 flakes that lack broken inversion symmetry are used as a dielectric layer has also been constructed as shown in Figure S1. It is clear that the hysteresis of such a device nearly disappears.

To obtain a high-performance device, a γ-InSe flake was directly selected as a conducting channel. Here, γ-InSe-based dual-gate SFeCT was fabricated as shown in Figure 2a, where the monolayer graphene was adopted as the source−drain electrodes due to its easily tunable Fermi level.[20] These individual flakes (graphite, monolayer graphene, h-BN, and γ-InSe) were prepared by micromechanical exfoliation first, and then they were sequentially assembled into a heterostructure by a standard dry transfer method.[21]

The transfer characteristics of the device modulated by the top gate and back gate are illustrated in Figure 2b,c, respectively, where the drain−source voltage (V_{ds}) is fixed as 1 V. When the device is tuned by the top gate as shown in Figure 2b, a memory window with clockwise hysteresis is obtained, and the memory window slightly increases from 0.5 to 1 V as the sweeping range of top-gate $|V_g|$ increases from 1 to 5 V. Similarly, when the device is modulated by the back gate, the transfer characteristic also presents a clockwise hysteresis, as shown in Figure 2c. However, the memory windows show an obviously increasing tendency as the sweeping range of back-gate voltage increases. The memory window can reach even up to 4.5 V, while the back-gate voltage sweeps from −5 to 5 V and back to −5 V. So far, the memory window tuned by the top gate and back gate shows an obviously different behavior.

To rule out the possibility that charge-trapping effects generate a similar hysteric behavior, different scanning rates of sweeping back-gate voltage were set. It is well-known that charge trapping effects can be distinguished via using different scanning rates, which has been widely used in the graphene device.[22] As shown in Figure 2d, the clockwise hysteresis loop and the memory windows are independent of the different gate scanning rates, strongly indicating that the charge-trapping effects do not play a role in the hysteretic behavior of SFeCT.

It is worth noting that an obvious nonlinear behavior was found in the output curve (cyan dotted line), indicating the formation of a Schottky barrier in the graphene/γ-InSe/graphene junction, as shown in Figure 2e. This is in contrast to the previously reported ferroelectric semiconductor devices based on α-In_2Se_3[23] or Bi_2O_2Se,[24] where ohmic contact forms between the channel and electrode. Actually, in back-to-back Schottky barrier-based devices, one of the Schottky diodes always presents a reverse configuration regardless of the sign of drain voltage (detailed discussion in Figure S3).[25,26] This is the reason the current at a positive V_{ds} approaches saturation. In

https://doi.org/10.1021/acs.nanolett.3c01053
Nano Lett. 2023, 23, 4595−4601

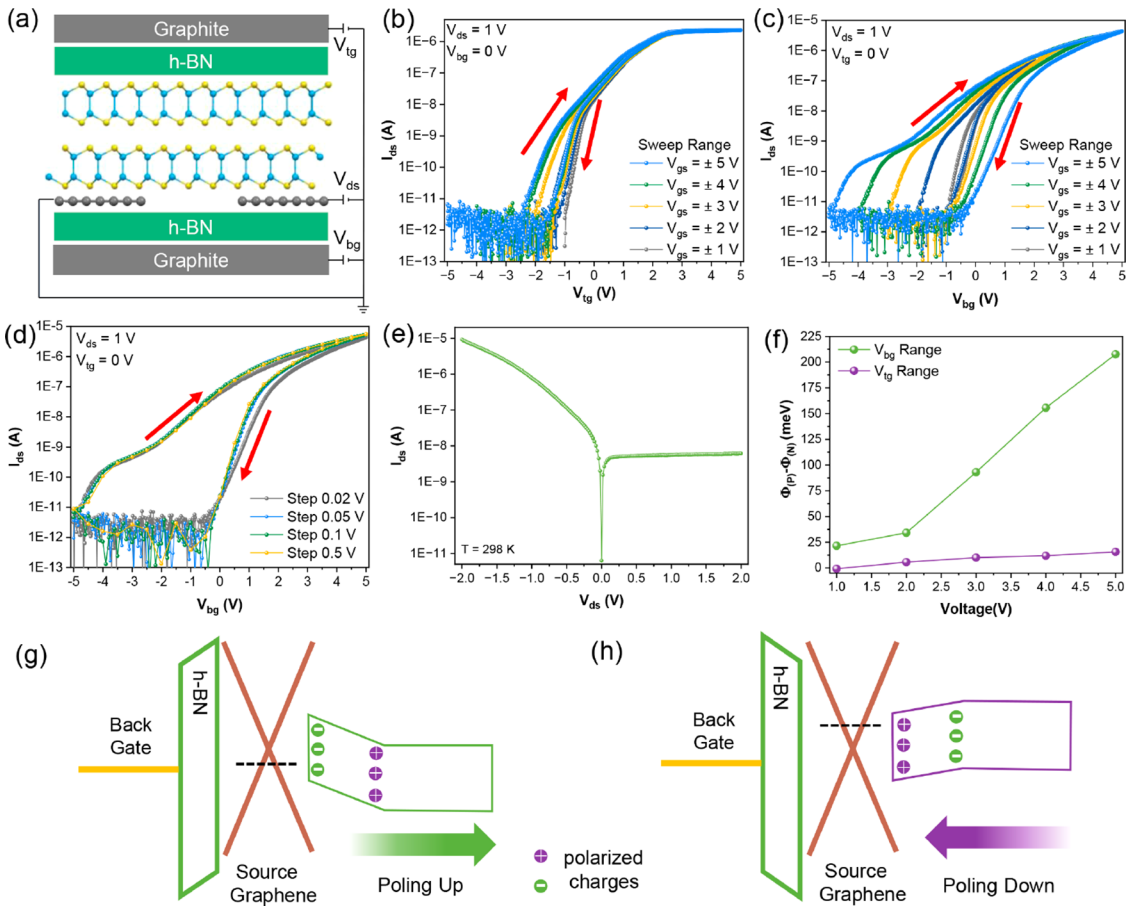


Figure 2. (a) Illustration of a device structure of SFeCT. (b) and (c) Transfer characteristic ($I_d - V_{tg(bg)}$) of SFeCT with different sweep ranges at a fixed drain voltage of 1 V. (d) Transfer characteristic ($I_d - V_{bg}$) of SFeCT with different sweep rates at a fixed drain voltage of 1 V. (e) Output characteristic ($I_d - V_{ds}$) of SFeCT with a grounded gate bias ($V_{bg(tg)}$ = 0 V). (f) Variation of Schottky barrier extracted according to (b) and (c). (g) and (h) Band diagram of SFeCT in polarization up and polarization down states (black dashed line represents the Fermi level of graphene), respectively.

addition, the near flat source−drain current at a V_{tg} above 2.5 V also suggests that the contact resistance plays a key role in the performance of the device (Figure 2b and Figure S4). Therefore, the current of the device at V_{ds} = 1 V is dominated by the reversed junction at the source terminal of graphene/γ-InSe. Based on the thermionic emission model, the height of the barrier can be accurately extracted. Most importantly, taking advantage of the source−drain current at positive or negative gate voltage enables the quantitative calculation of the relative change of Schottky barrier ($\Phi_P - \Phi_N$). The results are depicted in Figure 2f. One can see that $\Phi_P - \Phi_N$ sharply increases with the increasing back-gate voltage (V_{bg}) but slightly increases with the top-gate voltage (V_{tg}). In other words, the V_{bg} could induce an obvious switching of Schottky barriers in the forward and backward sweeping direction, while the switching of Schottky barriers induced by V_{tg} is pretty weak. As a result, a much smaller memory window tuned by top gate compared to the back gate is observed.

Based on the above analysis, a ferroelectricity-associated operation mechanism is proposed, where the ferroelectric polarization provides an efficient way to modulate the Schottky barriers. The band diagrams are presented in Figure 2g and h. Specifically, when a positive back-gate voltage is applied, the positive polarization in γ-InSe with upward direction is formed. After the back-gate voltage is withdrawn or set to zero, the negative polarized charges at the bottom of γ-InSe remained. A part of these negative polarized charges could be screened by holes in γ-InSe, while the unscreened negative polarized charges could further induce extra holes in graphene due to the electrostatic effect. As a result, the Fermi level of graphene decreases, and the height of the Schottky barrier between graphene and γ-InSe is improved, in which the off-state of γ-InSe-based SFeCT occurs. Conversely, after a negative back-gate voltage is applied, the positive polarized charges are left behind at the bottom of γ-InSe. The extra electrons are then induced at both graphene and γ-InSe, raising the Fermi level of graphene and reducing the Schottky barriers of graphene/γ-InSe, which means γ-InSe-based SFeCT is at the on state. So far, electrically tuning the ferroelectric polarization by a back gate indirectly achieves a memory state switching. In principle, the memory behaviors of SFeCT root in the polarization switching and the corresponding induced redistribution of mobile carriers. Nevertheless, the strength of the electric field penetrating into the channel to switch the polarization should be strongly related with carrier concentration of the ferroelectric semiconductor. For example, when the SFeCT is controlled by the top gate, the Schottky barrier at V_{tg} = 0 V is nearly equivalent regardless of V_{tg} sweeping from −5 to 0 V or from 5 to 0 V, while an obvious memory window shows at a negative top-gate voltage, indicating the height of the Schottky barrier is changed. Therefore, it suggests that reducing the carrier concentration of γ-InSe provides an efficient way to

https://doi.org/10.1021/acs.nanolett.3c01053
Nano Lett. 2023, 23, 4595−4601

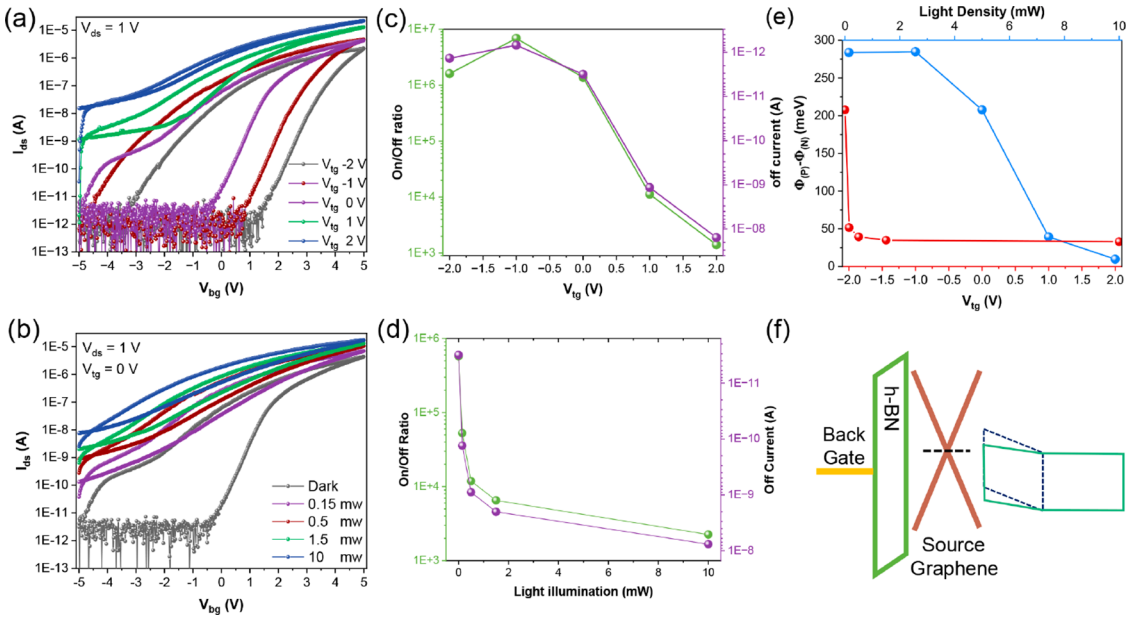


Figure 3. (a) Transfer characteristics ($I_d - V_{bg}$) of SFeCT applying different top gates. (b) Transfer characteristics ($I_d - V_{bg}$) of SFeCT under different intensities of 532 nm laser illumination. (c) and (d) On/off ratio and off-state current as a function of top gate and light illumination. (e) Variation of the Schottky barrier under top gate or light illumination, which shows a decreasing variation of the Schottky barrier. (f) Schematic of the top gate or light tuning the Schottky barrier (blue dashed line is the initial barrier, black dashed line is the Fermi level of graphene, and the blue line represents the Schottky barrier after electron doping).

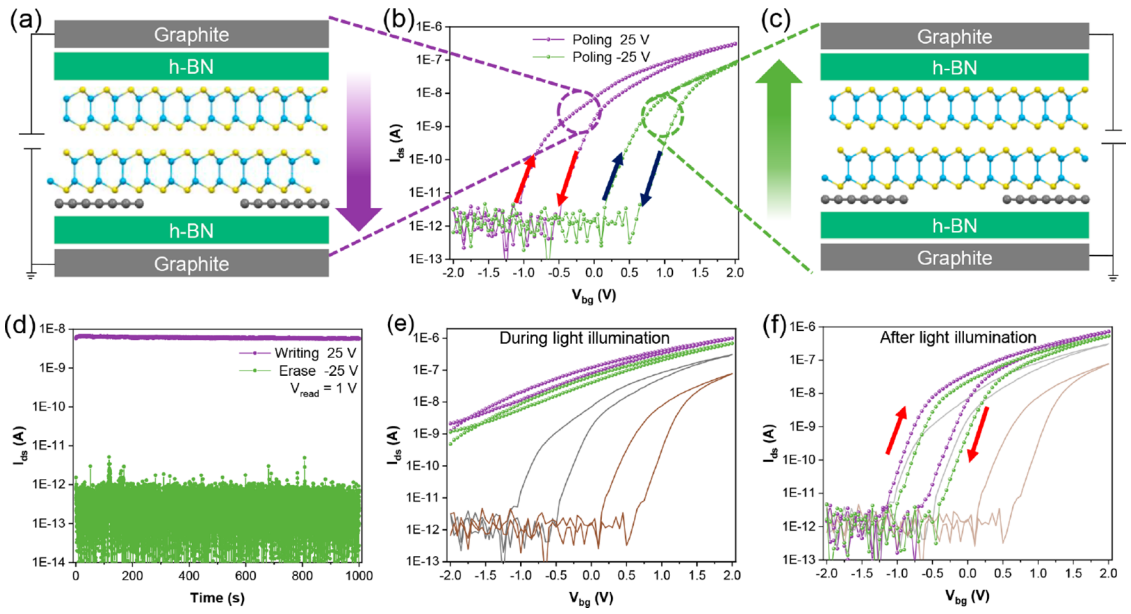


Figure 4. (a) Illustration of polarization down by the top gate. During the programming operation, a positive voltage is applied on the top gate, while the back gate is grounded. (b) The transfer characteristics ($I_d - V_{bg}$) of SFeCT after various program voltages (±25 V) at 250 K. (c) Illustration of polarization up by the top gate. During the programming operation, a negative voltage is applied on the top gate as the back gate is grounded. (d) The retention of different states of SFeCT for 1000 s after ±25 V programming by the top gate. (e) Transfer characteristics ($I_d - V_{bg}$) of SFeCT during light illumination. (f) Transfer characteristics ($I_d - V_{bg}$) of SFeCT after light illumination (the dark and brown lines represent the transfer characteristics before light illumination).

enhance the polarization switching. Furthermore, it can be rationally inferred that the polarization switching process mainly occurs in the area of the γ-InSe channel overlapped with dielectrics, where the carrier concentration is enough to screen the external electric field. This is similar to the incomplete polarization switching in α-In_2Se_3.[23]

To verify the above mechanism and obtain a tunable memory window as well as a flexible on/off ratio, electrostatic doping and light illumination were adopted to tune the carrier concentration, respectively. The experimental results are displayed in Figure 3a,b. The extracted on/off ratio is illustrated in Figure 3c,d. For electrostatic doping, when V_{tg} is set as −2 V to reduce the intrinsic electron concentration in γ-InSe, the memory window expands to 5 V. However, when V_{tg} is set as 2 V to largely improve electron concentration, the memory windows almost disappear, and the on/off ratio

https://doi.org/10.1021/acs.nanolett.3c01053
Nano Lett. 2023, 23, 4595−4601

decreases down to 10^3. For light illumination, the transfer characteristic of the device shows a similar changing tendency, where the memory window shrinks and the on/off ratio decreases to about 10^3 as the power of illumination increases. When a positive V_{tg} or illumination is applied, a large number of mobile carriers will be generated, and γ-InSe becomes more conductive. Therefore, when a sweeping back-gate voltage is applied, the polarized charges on the bottom of γ-InSe are well screened by the channel itself. Meanwhile, the changing of graphene Fermi level associated with polarization switching is negligible, and thus the $\Phi_P - \Phi_N$ of the graphene/γ-InSe junction decreases as shown in Figure 3e. The relative energy band diagram is depicted in Figure 3f. When sweeping the top gate voltage, a more negative back-gate voltage is needed to reduce the electron concentration to achieve the Schottky barrier switching (see Figure S5).

In the γ-InSe-based SFeCT device, the electronic transportation is mainly determined by the reversed Schottky junction between graphene and γ-InSe, and the Schottky barrier can be further modulated by the ferroelectric polarization. Thus, to improve the on/off ratio of the memory states, it is necessary to enhance the dissimilarity of the barrier height between the on-state and off-state. Considering the effect of ferroelectric polarization on the Fermi level of graphene, the completed polarization switching is an efficient way to facilitate the accumulation of free carriers in graphene. Here, a strong electric field vertically across the channel is adopted to switch the polarization, where the source and drain terminal of the device is floated as shown in Figure 4a,c. After being programmed by a large voltage (25 V or −25 V), the transfer characteristics of the device modulated by the back gate are displayed in Figure 4b. It is found that the off-state voltage at downward polarization states shifts more than 1 V when compared with the case at upward polarization states. As a result, the SFeCT shows a large memory window and a moderate on/off ratio of about 10^4. Notably, the shifts of off-state voltage or memory windows present an increasing tendency as the poling voltage increases (Figure S6). Most importantly, benefiting from the completed polarization switching, the retention property of different states is also enhanced. As shown in Figure 4d, the on/off ratio of memory states almost stays at 10^4 for 1000 s after programming by the top gate voltage of ±25 V. Moreover, the memory states could also be well removed by applying light illumination. As shown in Figure 4f, after withdrawing the light, the off-state voltage of the device is all around −1 V regardless of whether a +25 V or −25 V programmed pulse voltage has been applied previously.

In summary, the sliding ferroelectricity in the narrow bandgap semiconductor γ-InSe has been demonstrated. The semiconducting nature of γ-InSe enables the fabrication of ferroelectric channel transistors with high-performance nonvolatile memory properties. The device shows a large memory window and a high on/off ratio, with good retention time. The working mechanism of our proposed device lies in the ferroelectric polarization modulating Schottky barrier height change. Furthermore, the device performance could be adjusted via the free carrier doping induced by gating voltage or light excitation, which is essential for designing novel in-sensor/in-memory processing architectures. We believe that the γ-InSe-based sliding ferroelectric transistor is a promising candidate for the emerging memory and computing applications.

METHODS

Device Fabrication. The individual flakes of graphite, h-BN, and monolayer graphene were mechanically exfoliated onto the silicon chip covered with a 285 nm SiO_2 at atmosphere. Two monolayer graphene flakes, an h-BN, and a graphite were picked up by PDMS covered with polycarbonate in sequence under 70−90 °C, and then the back gate with electrodes was placed on the blank silicon chip at 180 °C. Subsequently, the silicon chip was immersed in chloroform solution overnight to remove the polycarbonate. For the top gate, the graphite was picked up first, and then an h-BN flake was picked up. Both parts were transferred into the glovebox. The bulk γ-InSe (from a 2D semiconductor) was exfoliated in a glovebox with an oxygen and water concentration below 0.1 ppm. A fresh γ-InSe flake was quickly picked up by part of the top gate, and then the assembly of the dual-gate device was realized. After the polymer was dissolved, a metal electrode (Cr 8 nm/Au 30 nm) was introduced on the dual-gate device followed by lithography and electron beam evaporation.

Electrical Measurement. The electric measurement of the device was conducted using a FS-Pro 380 semiconductor parameter analyzer. Variable-temperature measurement was performed in a cryostation (Montana Instrument).

STEM. The sample of γ-InSe was made by drop casting. The atomic resolution ADF-STEM imaging was performed on an aberration-corrected ARM200F, equipped with a cold field-emission gun operating at 80 kV.

Variation of Schottky Barrier Extraction. The variation of the Schottky barrier between P (positive back gate) and N (negative back gate) was extracted based on the thermionic theory, and it is simplified by the following equation[27,28]

$$\ln[I(\mathrm{P})/I(\mathrm{N})] \sim -q(\Phi_P - \Phi_N)/kT$$

where $I(\mathrm{P})$ and $I(\mathrm{N})$, respectively, are the current under the 1 V drain voltage a at zero back gate; q is the magnitude of the electron charge; k is the Boltzmann constant; and T is the temperature.

ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acs.nanolett.3c01053.

Transfer curve of graphene with a 2H-MoS_2 flake as a dielectric layer; the electric transport of graphene with a γ-InSe flake as a dielectric layer; the detailed discussion of the output curve of SFeCT; top and back gate transfer curve under different drain voltages; top gate transfer curve of SFeCT under electrostatic doping and light illumination; top and back gate transfer curve of SFeCT under different drain voltages; back gate electric transport of SFeCT after different top gate program voltage and the output curve of SFeCT at 50 K (PDF)

AUTHOR INFORMATION

Corresponding Authors

Qing Liu − *School of Optoelectronic Science and Engineering, University of Electronic Science and Technology of China, Chengdu 611731, China*; Email: liuqing19@uestc.edu.cn

Xiaoxu Zhao − *School of Materials Science and Engineering, Peking University, Beijing 100871, China*; orcid.org/0000-0001-9746-3770; Email: xiaoxuzhao@pku.edu.cn

https://doi.org/10.1021/acs.nanolett.3c01053
Nano Lett. 2023, 23, 4595−4601

Wenwu Li − *Shanghai Frontiers Science Research Base of Intelligent Optoelectronics and Perception, Institute of Optoelectronics, Department of Materials Science, Fudan University, Shanghai 200433, China;* orcid.org/0000-0002-9307-1566; Email: liwenwu@fudan.edu.cn

Fucai Liu − *School of Optoelectronic Science and Engineering, University of Electronic Science and Technology of China, Chengdu 611731, China; Yangtze Delta Region Institute (Huzhou), University of Electronic Science and Technology of China, Huzhou 324003, China; State Key Laboratory of Electronic Thin Films and Integrated Devices, University of Electronic Science and Technology of China, Chengdu 611731, China;* orcid.org/0000-0003-1275-0573; Email: fucailiu@uestc.edu.cn

Authors

Renji Bian − *School of Optoelectronic Science and Engineering, University of Electronic Science and Technology of China, Chengdu 611731, China; Yangtze Delta Region Institute (Huzhou), University of Electronic Science and Technology of China, Huzhou 324003, China*

Guiming Cao − *School of Information Science and Technology, Xi Chang University, Xi Chang 615013, China*

Er Pan − *School of Optoelectronic Science and Engineering, University of Electronic Science and Technology of China, Chengdu 611731, China*

Zefen Li − *School of Optoelectronic Science and Engineering, University of Electronic Science and Technology of China, Chengdu 611731, China*

Lei Liang − *School of Optoelectronic Science and Engineering, University of Electronic Science and Technology of China, Chengdu 611731, China*

Qingyun Wu − *Science, Mathematics and Technology, Singapore University of Technology and Design (SUTD), Singapore 487372, Singapore*

Lay Kee Ang − *Science, Mathematics and Technology, Singapore University of Technology and Design (SUTD), Singapore 487372, Singapore;* orcid.org/0000-0003-2811-1194

Complete contact information is available at: https://pubs.acs.org/10.1021/acs.nanolett.3c01053

Notes

The authors declare no competing financial interest.

■ ACKNOWLEDGMENTS

This work was supported by the National Natural Science Foundation of China (Nos. 12161141015, 62074025, and 52002051), the National Key Research & Development Program (Nos. 2021YFE0194200 and 2020YFA0309200), and Sichuan Province Key Laboratory of Display Science and Technology. This work was also supported by the Fundamental Research Funds for the Central Universities, SCUT (No. ZYGX2020J009), and the Applied Basic Research Program of Sichuan Province (2021JDGD0026). Q.Y.W. and L.K.A. were supported by Singapore A*STAR AME IRG (A2083c0057). X.X.Z. thanks the National Natural Science Foundation of China (Grant No. 52273279), and the Beijing Natural Science Foundation (Grant No. Z220020)

■ REFERENCES

(1) Li, L.; Wu, M. Binary compound bilayer and multilayer with vertical polarizations: two-dimensional ferroelectrics, multiferroics, and nanogenerators. *ACS Nano* **2017**, *11* (6), 6382−6388.

(2) Wu, M. Two-dimensional van der Waals ferroelectrics: Scientific and technological opportunities. *ACS Nano* **2021**, *15* (6), 9229−9237.

(3) Yasuda, K.; Wang, X.; Watanabe, K.; Taniguchi, T.; Jarillo-Herrero, P. Stacking-engineered ferroelectricity in bilayer boron nitride. *Science* **2021**, *372* (6549), 1458−1462.

(4) Woods, C.; Ares, P.; Nevison-Andrews, H.; Holwill, M.; Fabregas, R.; Guinea, F.; Geim, A.; Novoselov, K.; Walet, N.; Fumagalli, L. Charge-polarized interfacial superlattices in marginally twisted hexagonal boron nitride. *Nat. Commun.* **2021**, *12* (1), 347.

(5) Vizner Stern, M.; Waschitz, Y.; Cao, W.; Nevo, I.; Watanabe, K.; Taniguchi, T.; Sela, E.; Urbakh, M.; Hod, O.; Ben Shalom, M. Interfacial ferroelectricity by van der Waals sliding. *Science* **2021**, *372* (6549), 1462−1466.

(6) Rogée, L.; Wang, L.; Zhang, Y.; Cai, S.; Wang, P.; Chhowalla, M.; Ji, W.; Lau, S. P. Ferroelectricity in untwisted heterobilayers of transition metal dichalcogenides. *Science* **2022**, *376* (6596), 973−978.

(7) Meng, P.; Wu, Y.; Bian, R.; Pan, E.; Dong, B.; Zhao, X.; Chen, J.; Wu, L.; Sun, Y.; Fu, Q.; et al. Sliding induced multiple polarization states in two-dimensional ferroelectrics. *Nat. Commun.* **2022**, *13* (1), 7696.

(8) Deb, S.; Cao, W.; Raab, N.; Watanabe, K.; Taniguchi, T.; Goldstein, M.; Kronik, L.; Urbakh, M.; Hod, O.; Ben Shalom, M. Cumulative polarization in conductive interfacial ferroelectrics. *Nature* **2022**, *612* (7940), 465−469.

(9) Jindal, A.; Saha, A.; Li, Z.; Taniguchi, T.; Watanabe, K.; Hone, J. C.; Birol, T.; Fernandes, R. M.; Dean, C. R.; Pasupathy, A. N.; Rhodes, D. A. Coupled ferroelectricity and superconductivity in bilayer Td-$MoTe_2$. *Nature* **2023**, *613* (7942), 48−52.

(10) Klein, D. R.; Xia, L.-Q.; MacNeill, D.; Watanabe, K.; Taniguchi, T.; Jarillo-Herrero, P. Electrical switching of a bistable moiré superconductor. *Nat. Nanotechnol.* **2023**, *18*, 331−335.

(11) Kang, K.; Zhao, W.; Zeng, Y.; Watanabe, K.; Taniguchi, T.; Shan, J.; Mak, K. F. Switchable moiré potentials in ferroelectric WTe_2/WSe_2 superlattices. *Nat. Nanotechnol.* **2023**, DOI: 10.1038/s41565-023-01376-5.

(12) Weston, A.; Castanon, E. G.; Enaldiev, V.; Ferreira, F.; Bhattacharjee, S.; Xu, S.; Corte-León, H.; Wu, Z.; Clark, N.; Summerfield, A.; et al. Interfacial ferroelectricity in marginally twisted 2D semiconductors. *Nat. Nanotechnol.* **2022**, *17* (4), 390−395.

(13) Sui, F.; Jin, M.; Zhang, Y.; Qi, R.; Wu, Y.-N.; Huang, R.; Yue, F.; Chu, J. Sliding ferroelectricity in van der Waals layered γ-InSe semiconductor. *Nat. Commun.* **2023**, *14* (1), 36.

(14) Feng, W.; Zheng, W.; Cao, W.; Hu, P. Back gated multilayer InSe transistors with enhanced carrier mobilities via the suppression of carrier scattering from a dielectric interface. *Adv. Mater.* **2014**, *26* (38), 6587−6593.

(15) Bandurin, D. A.; Tyurnina, A. V.; Yu, G. L.; Mishchenko, A.; Zólyomi, V.; Morozov, S. V.; Kumar, R. K.; Gorbachev, R. V.; Kudrynskyi, Z. R.; Pezzini, S.; et al. High electron mobility, quantum Hall effect and anomalous optical response in atomically thin InSe. *Nat. Nanotechnol.* **2017**, *12* (3), 223−227.

(16) Zhang, B.; Wu, H.; Peng, K.; Shen, X.; Gong, X.; Zheng, S.; Lu, X.; Wang, G.; Zhou, X. Super deformability and thermoelectricity of bulk γ-InSe single crystals. *Chinese Phys. B* **2021**, *30* (7), 078101.

(17) Fei, Z.; Zhao, W.; Palomaki, T. A.; Sun, B.; Miller, M. K.; Zhao, Z.; Yan, J.; Xu, X.; Cobden, D. H. Ferroelectric switching of a two-dimensional metal. *Nature* **2018**, *560* (7718), 336−339.

(18) Wang, X.; Yasuda, K.; Zhang, Y.; Liu, S.; Watanabe, K.; Taniguchi, T.; Hone, J.; Fu, L.; Jarillo-Herrero, P. Interfacial ferroelectricity in rhombohedral-stacked bilayer transition metal dichalcogenides. *Nat. Nanotechnol.* **2022**, *17* (4), 367−371.

(19) Xue, J.; Sanchez-Yamagishi, J.; Bulmash, D.; Jacquod, P.; Deshpande, A.; Watanabe, K.; Taniguchi, T.; Jarillo-Herrero, P.; LeRoy, B. J. Scanning tunnelling microscopy and spectroscopy of

ultra-flat graphene on hexagonal boron nitride. *Nat. Mater.* **2011**, *10* (4), 282−285.
(20) Wu, J.; Chen, H.-Y.; Yang, N.; Cao, J.; Yan, X.; Liu, F.; Sun, Q.; Ling, X.; Guo, J.; Wang, H. High tunnelling electroresistance in a ferroelectric van der Waals heterojunction via giant barrier height modulation. *Nat. Electron.* **2020**, *3* (8), 466−472.
(21) Purdie, D.; Pugno, N.; Taniguchi, T.; Watanabe, K.; Ferrari, A.; Lombardo, A. Cleaning interfaces in layered materials heterostructures. *Nat. Commun.* **2018**, *9* (1), 5387.
(22) Wang, H.; Wu, Y.; Cong, C.; Shang, J.; Yu, T. Hysteresis of electronic transport in graphene transistors. *ACS Nano* **2010**, *4* (12), 7221−7228.
(23) Si, M.; Saha, A. K.; Gao, S.; Qiu, G.; Qin, J.; Duan, Y.; Jian, J.; Niu, C.; Wang, H.; Wu, W.; et al. A ferroelectric semiconductor field-effect transistor. *Nat. Electron.* **2019**, *2* (12), 580−586.
(24) Wang, W.; Meng, Y.; Zhang, Y.; Zhang, Z.; Wang, W.; Lai, Z.; Xie, P.; Li, D.; Chen, D.; Quan, Q.; et al. Electrically Switchable Polarization in Bi_2O_2Se Ferroelectric Semiconductors. *Adv. Mater.* **2023**, *35*, 2210854.
(25) Di Bartolomeo, A.; Grillo, A.; Urban, F.; Iemmo, L.; Giubileo, F.; Luongo, G.; Amato, G.; Croin, L.; Sun, L.; Liang, S.-J.; Ang, L. K. Asymmetric Schottky contacts in bilayer MoS_2 field effect transistors. *Adv. Funct. Mater.* **2018**, *28* (28), 1800657.
(26) Marquez, C.; Salazar, N.; Gity, F.; Navarro, C.; Mirabelli, G.; Galdon, J. C.; Duffy, R.; Navarro, S.; Hurley, P. K.; Gamiz, F. Investigating the transient response of Schottky barrier back-gated MoS_2 transistors. *2D Mater.* **2020**, *7* (2), 025040.
(27) Xue, F.; He, X.; Retamal, J. R. D.; Han, A.; Zhang, J.; Liu, Z.; Huang, J. K.; Hu, W.; Tung, V.; He, J. H.; et al. Gate-tunable and multidirection-switchable memristive phenomena in a van der Waals ferroelectric. *Adv. Mater.* **2019**, *31* (29), 1901300.
(28) Zhou, J.; Fei, P.; Gu, Y.; Mai, W.; Gao, Y.; Yang, R.; Bao, G.; Wang, Z. L. Piezoelectric-potential-controlled polarity-reversible Schottky diodes and switches of ZnO wires. *Nano Lett.* **2008**, *8* (11), 3973−3977.

https://doi.org/10.1021/acs.nanolett.3c01053
Nano Lett. 2023, 23, 4595−4601